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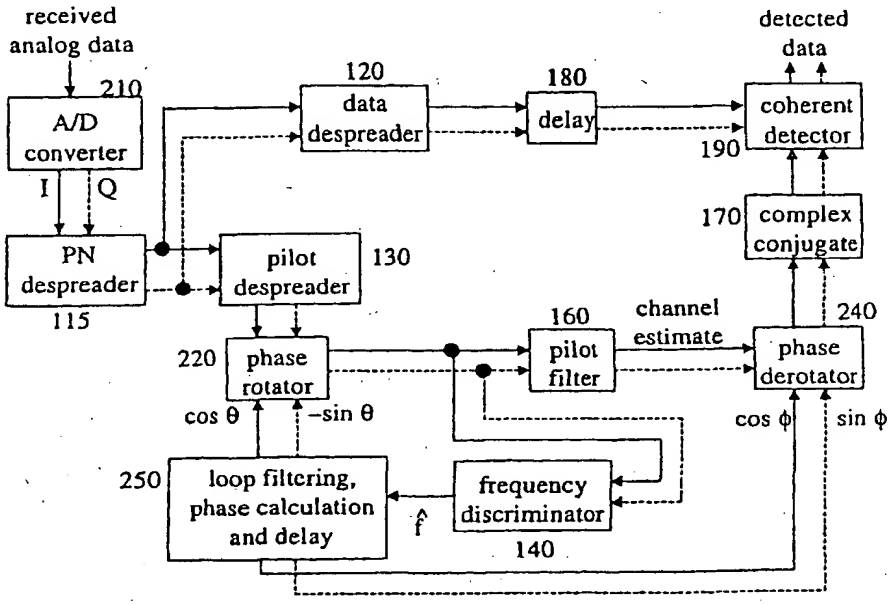


(57) Abstract

Coherent detection of high-speed digital wireless communications becomes more difficult when the frequencies of the transmitter and receiver oscillators do not coincide. A frequency-locked loop may be used to characterize this frequency offset by processing the samples received on a pilot channel. Rather than using the offset information thus derived to correct the frequency of the received signal, the invention realizes considerable computational savings by applying a frequency correction to the despread pilot samples instead.

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# METHOD AND APPARATUS FOR FREQUENCY OFFSET CORRECTION

## BACKGROUND OF THE INVENTION

### I. Field of the Invention

This invention relates to wireless communications. More specifically, this invention relates to systems for digital wireless communications that employ coherent detection.

### II. Description of Related Art and General Background

1) Spread spectrum and code-division multiple-access

Spread spectrum communication techniques are robust to noise, allow for the use of low transmission power, and have a low probability of intercept. For such reasons, much of the early development of spread spectrum technology was performed by military researchers. Recently, however, the advantages of this technology have led to its increasing use for consumer applications as well: most notably, in advanced digital cellular telephone systems.

Whereas most other communication techniques modulate a carrier signal with one or more data signals alone, spread spectrum techniques also modulate the carrier with a pseudorandom noise or 'pseudonoise' (PN) signal. In the frequency-hopping variant of spread spectrum systems, the value of the PN signal at a particular instant determines the frequency of the transmitted signal, and thus the spectrum of the signal is spread. In the direct sequence spread spectrum (DSSS) variant, the bit rate of the PN signal (called the 'chip rate') is chosen to be higher than the bit rate of the information signal, such that when the carrier is modulated by both signals, its spectrum is spread.

Communication systems that support multiple individual signals over a single channel must employ some technique to make the various signals distinguishable at the receiver. In time-division multiple-access (TDMA) systems, the individual signals are transmitted in nonoverlapping intervals such that they are orthogonal (and thus separable) in time space. In frequency-division multiple-access (FDMA) systems, the signals are bandlimited and transmitted in nonoverlapping subchannels such that they are orthogonal in

frequency space. In code-division multiple-access (CDMA) systems, the signals are spread through modulation by orthogonal or uncorrelated code sequences such that they are orthogonal or nearly orthogonal in code space and may be transmitted across the same channel at the same time while remaining distinguishable from one another at the receiver. An exemplary CDMA system is described in U.S. Patent No. 4,901,307, entitled "SPREAD SPECTRUM MULTIPLE-ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS," issued February 13, 1990 and assigned to the assignee of the present invention, and the disclosure of which is hereby incorporated by reference.

In a CDMA DSSS system, then, each individual carrier signal is modulated by a data signal and a pseudonoise (PN) signal that is at least nearly orthogonal to the PN signals assigned to all other users, thus spreading the spectrum of the transmitted signal while rendering it distinguishable from the other users' signals. Before spreading and modulation onto the carrier, the data signal typically undergoes various encoding and interleaving operations designed, for example, to increase data redundancy and allow error correction at the receiver. The data signals may also be encrypted to provide extra security against eavesdroppers. The generation of CDMA signals in a spread spectrum communications system is disclosed in U.S. Patent No. 5,103,459, entitled "SYSTEM AND METHOD FOR GENERATING SIGNAL WAVEFORMS IN A CDMA CELLULAR TELEPHONE SYSTEM," issued April 7, 1992 and assigned to the assignee of the present invention, and the disclosure of which is hereby incorporated by reference.

2) Phase modulation

In a DSSS telecommunications system, the baseband information signal is typically spread by the PN sequences to have a bandwidth of 1 MHz or more. In order to transmit the spread baseband signal over a radio channel, it is necessary to modulate it onto an RF carrier of the desired frequency.

Various methods of modulating digital baseband signals onto RF carriers exist. These methods typically operate by varying the amplitude, phase, and/or frequency of one or both of the in-phase (I) and quadrature (Q) components of the carrier according to the data symbol to be transmitted at any particular instant. DSSS systems commonly use a variant of either phase-shift keying (PSK), in which the phase states in the carrier components correspond to data symbols being transferred, or quadrature amplitude modulation (QAM),

in which both the phases and the amplitudes of the carrier components are modulated.

In an exemplary system using binary PSK (BPSK) modulation, a transition of the carrier from a base phase state (defining a phase of zero) to a second phase state which is different by 180 degrees (i.e. a phase shift of $\pi$ radians away from zero) may be designated to indicate a transition from a data symbol 0 to a data symbol 1. The converse phase shift of $\pi$ radians back to zero would then be designated to indicate a transition from a data symbol 1 to a data symbol 0. Between these transitions, the phase of the carrier indicates whether a data symbol 0 is being transmitted (phase of zero) or a data symbol 1 instead (phase of $\pi$ radians). An improved ratio of data rate to bandwidth may be obtained by using quadrature PSK (QPSK) modulation, in which the data symbols are encoded into 180-degree shifts in both the I and Q components. These and other variants of PSK modulation are well known in the art.

Note that in PSK modulation, all phase states have significance only in relation to the base phase state. If this reference state is unknown, then only the points of phase state transition may be identified, and the actual identities of the symbols cannot be determined. In the BPSK system described above, for example, a phase shift of $\pi$ radians indicates either a transition from 0 to 1 or from 1 to 0. Unless one knows the relation between the base phase state and either the starting or the ending phase state, it is impossible to determine which transition was meant.

This phase ambiguity problem may be addressed in several different ways. One approach has been to avoid it by using a modulation which is suitable for noncoherent detection and does not require knowledge of the base phase state, such as differential PSK (DPSK). A more power-efficient method uses orthogonal signalling sets to encode the data symbols in a manner which is unambiguous regardless of the base phase state. The Hadamard-Walsh functions are one suitable signalling set, as discussed in Chapter 4 of *CDMA: Principles of Spread Spectrum Communications* by Andrew J. Viterbi, Addison Wesley Longman, Reading, MA, 1995, which chapter is herein incorporated by reference. However, by providing the informational redundancy necessary to avoid the phase ambiguity problem, these methods may also reduce the achievable data throughput of the channel. An alternative approach has been to use a coherent detection scheme.

3) Coherent detection and phase noise

In pilot-assisted coherent detection, the base phase state is derived from a pilot signal, a signal of known form which is transmitted along with the data signal to provide a phase and magnitude reference. One method of transmitting pilot and data channels over the same carrier is to cover the channels with different orthogonal codes (e.g., with different Walsh functions). At the receiver, the pilot channel may be used to establish carrier synchronization and enable coherent detection by, for example, using a phase-locked loop to keep the output of a local oscillator at a constant phase angle with respect to the received pilot.

Unfortunately, carrier synchronization is often complicated by the presence of phase noise. Phase noise may have two components, one being random and the other being more determinable. The random component is primarily due to Doppler effects caused by relative motion between the transmitter and receiver (or apparent motion between the two, as might be caused by a reflector). The maximum magnitude $f_{d\_max}$ of such a Doppler shift is defined as

$f_{d\_max} = f_c \times v / c,$

where $f_c$ is the carrier frequency in Hz, v is the relative velocity in m/sec, and c is the speed of light. For carrier frequencies in the gigahertz range and relative velocities of a few hundred miles per hour, the Doppler component may be on the order of hundreds of Hertz.

Because the Doppler component changes rapidly and may exceed a few percent of the data rate, it is typically very difficult to track using a phase-locked loop. An alternative way to compensate for this random component is to use the known pilot signal to obtain an estimate of the channel's effects. This estimate is usually in the form of a complex vector which represents the rotation in phase introduced by the channel and is used to compensate for the same rotation in the data samples.

Phase noise also arises as a frequency offset within the system architecture, caused primarily by a difference in frequency between the oscillators in the transmitter and the receiver. This difference may arise, for example, because of variances in manufacture or drift due to aging or temperature, and the effect of this offset is to introduce a phase rotation into the samples which remains relatively constant with respect to time. Section 10.1.1.3 of the IS-98A standard (TIA/EIA, July 1996) allows the frequency of the mobile station's carrier to have an error of as much as 300 Hz once the oscillators have been phase-locked.

If the constant-rotating-component frequency offset is compensated separately, then a much better estimate of the random component of the phase noise may be obtained. One method of correcting the frequency offset is by using a digital frequency-locked loop (DFLL). The elements and principles of operation of digital frequency-locked loops are well known in the art and are described, for example, in "Convergence and Output MSE of Digital Frequency-Locked Loop for Wireless Communications" by the inventor Ling, *Proceedings of the 1996 IEEE Vehicular Technology Conference*, Atlanta, pp. 1215–1219, and "AFC Tracking Algorithms" by Francis D. Natali, *IEEE Transactions on Communications*, vol. COM-32, no. 8, August 1984, pp. 935–947, which documents are hereby incorporated by reference.

Frequency offset correction

FIG. 1 illustrates one method of frequency offset correction that uses a DFLL. An RF stage (not shown) supplies received analog data to conversion and correction block 110 for A/D conversion and frequency correction. As detailed below, the frequency correction operation may be performed either before or after A/D conversion. The digitized and corrected in-phase (I) and quadrature (Q) sample streams are despread by PN spreader 115 and then by data despreader 120 and pilot despreader 130 to obtain the symbols of the data and pilot channels, respectively.

Frequency discriminator 140 receives the despread pilot samples and generates an instantaneous frequency error $\hat{f}$. As illustrated in FIG. 2, the value $\hat{f}$ is calculated as the imaginary portion of the complex product of the current pilot sample and the complex conjugate of the previous pilot sample. In loop filter 150, the instantaneous frequency error $\hat{f}$ is scaled to control the convergence and bandwidth of the DFLL and then integrated to obtain a more accurate offset frequency estimate $\tilde{f}$. This estimate of offset frequency is input to block 110 and used to adjust the phase of the received data.

In block 110, frequency correction may be applied in the analog domain by inputting analog data at RF or IF and using a voltage-controlled oscillator (VCO) controlled by the DFLL to downconvert the signal to baseband before A/D conversion. While it is relatively easy to perform frequency correction on an analog signal, however, for some applications it is not practical. For example, the signal received by a CDMA base station will typically contain signals from many users, each component signal having a different frequency offset. For a TDMA base station, the signal received during each time slot will typically come from a different user and have a different frequency offset than

the signal received in adjacent time slots. In such cases, it is preferable to perform the frequency correction in the digital domain. Moreover, better temperature stability and reliability of operation can be obtained in a smaller circuit area if the correction is performed digitally instead.

Frequency correction may be applied in the digital domain by inputting analog data to block 110 at baseband and applying complex rotations to the samples after A/D conversion. One disadvantage to performing the correction after digitization is that it becomes more intensive, requiring a complex rotation to be performed on every sample. For a typical chip rate of 1.2288 Mcps and a sampling rate of twice the chip rate, this method would require nearly 2.5 million complex rotations to be performed every second. The power and available area required to support such a processing rate renders digital frequency correction infeasible for many applications.

## SUMMARY OF THE INVENTION

By performing frequency correction processing on the pilot channel after despreading, rather than on the received samples before despreading, the invention considerably reduces the computational effort required to compensate for a frequency offset in the data channel. In order to maintain coherence between the data and pilot channels, the invention also includes derotating the channel estimate and delaying the samples in the data channel before coherent detection is performed.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a method of frequency correction.

FIG. 2 shows a circuit diagram for frequency discriminator 140.

FIG. 3 is a block diagram of the first embodiment of the invention.

FIG. 4 shows a circuit diagram for a quadricorrelator being a preferred implementation of frequency discriminator 140.

FIG. 5 shows a circuit diagram for a complex multiplier.

FIG. 6 illustrates a first implementation of loop filtering, phase calculation, and delay block 250.

FIG. 7 illustrates an implementation of frequency offset integrator 340.

FIG. 8A illustrates an implementation of phase adjustment integrator 350.

FIG. 8B illustrates a second implementation of phase adjustment integrator 350.

FIG. 9 illustrates a second implementation of loop filtering, phase calculation, and delay block 250.

FIG. 10 illustrates a first-order implementation of loop filter 325.

FIG. 11 illustrates a second-order implementation of loop filter 325.

FIG. 12 is a block diagram of an alternative embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 is a block diagram of the first embodiment of the invention. In a preferred implementation, the circuit of FIG. 3 (except for loop filtering, phase calculation, and delay block 250) would be replicated for several receivers, each receiving a different multipath instance of the signal from the same or different antennas. Such single-path receivers are commonly referred to as Rake 'fingers.' In such an implementation, loop filtering, phase calculation, and delay (LFPCD) block 250 would be common to all fingers, receiving a value $\hat{f}_i$ from each finger and outputting complex pairs $(\cos\theta, -\sin\theta)$ and $(\cos\phi, \sin\phi)$ in common to all fingers.

In the preferred embodiment of FIG. 3, the baseband analog data received from the RF and/or IF stages (not shown) passes through A/D converter 210, is despread by the PN sequence in PN despreader 115, and undergoes further despreading in data despreader 120 and pilot despreader 130. Despreaders 115 and 120 may be implemented as complex multipliers as illustrated in FIG. 5, where the inputs I_2 and Q_2 are the respective despreading codes. Assuming that the frequency offset is much lower than the data sample rate, the frequency offset may be ignored during the despreading operations.

In a preferred implementation, the pilot channel is covered by Walsh function 0 (i.e., the covering function is effectively a constant value). In this case, pilot despreader 130 may be implemented as an integrate-and-dump circuit. The integration period should be long in order to reduce the sample frequency and thus reduce the computational load, but on the other hand the integration period should be short so that the phase shift due to the frequency offset is negligible within that period. For a frequency offset of 300 Hz and a Doppler component of a few hundred Hertz, an integration period of about 200

μs is used for one embodiment. Before further processing, it may be desirable to truncate the pilot samples by right-shifting, for example. Truncation serves to reduce the data bitwidth in later stages, and a moderate amount of truncation and rounding at this stage has not been shown to introduce any performance degradation. However, truncation is optional.

After despreading, the pilot samples are rotated in phase rotator 220. A preferred implementation of phase rotator 220 is a complex multiplier, as shown in FIG. 5. The complex values which represent the angle of rotation θ are output by LFPCD block 250 as described below.

The rotated pilot samples are input to frequency discriminator 140, which outputs a measure $\hat{f}$ of the instantaneous frequency error. In a preferred implementation, frequency discriminator 140 (whose functionality is shown in FIG. 2) is implemented as a quadricorrelator as illustrated in FIG. 4.

FIG. 6 shows a block diagram of LFPCD block 250. As noted above, in a preferred implementation, a number of fingers individually calculate instantaneous frequency errors $\hat{f}_i$. These values are input to LFPCD block 250 through frequency error combiner 310. In a preferred implementation, combiner 310 outputs a value $\hat{f}_\Sigma$ as the sum of the values $\hat{f}_i$. However, combiner 310 may be constructed to output a weighted or non-weighted average of these values as well. If only one value of $\hat{f}$ is input to LFPCD block 250, combiner 310 may be omitted.

Limiter 320 provides a measure of system stability by restricting the possible range of the frequency error reported. In an alternative implementation, robustness is not necessary or is provided elsewhere. In such implementations, limiter 320 may be omitted.

Loop filter 325 receives the limited or non-limited frequency error value $\hat{f}_\Sigma$ (or $\hat{f}$, as appropriate) and outputs a frequency offset value $f_{off}$. FIG. 10 shows one implementation of a first-order filter suitable for use as loop filter 325. In this implementation, scaler 330 receives the input signal and outputs a scaled error value $\hat{f}_{SC}$. It is preferable to avoid multiplication in this stage by choosing a scaling factor of $2^{-n}$ and implementing scaler 330 as a right-shifter. As noted in the references incorporated above, for a first-order DFLL, the scaling factor determines the time constant of the DFLL (or, equivalently, its loop bandwidth) according to the following expression:

$T_c = NT_s / (\alpha k_d k_0)$,

where $T_c$ is the time constant of the DFLL in seconds; N is the insertion delay of the frequency discriminator and update interval of the loop filter in samples; $T_s$

is the sample period in seconds; $\alpha$ is the nondimensional scaling factor; $k_d$ is the gain of the frequency discriminator in LSB/Hz, where LSB denotes the least significant bit of the output of the frequency discriminator; and $k_0$ is the resolution of the phase rotation operation in Hz/LSB, where LSB denotes the least significant bit of the input to the digital-to-frequency converter (here, the input to lookup table 360). In a typical application, the scaling factor is the only factor in this expression that can be changed dynamically. (Parameters that may affect the values of the other factors in the expression above include the integration period, the signal-to-noise ratio, and the particular implementation of the digital-to-frequency converter.)

Of course, the scaling factor must also be chosen with regard to the number of fingers input to frequency error combiner 310 and the nature of combination performed therein (e.g. whether the inputs are averaged or simply accumulated). In order to keep the frequency error at the DFLL output below a desirable value, e.g., 100 Hz and ensure that this error will not degrade receiver performance, it is desirable for the time constant to be within the range from approximately 10 to approximately a few hundred milliseconds. In the exemplary application, typical values for the scaling factor range from approximately $2^2$ (4) to approximately $2^{-4}$ (1/16).

Frequency offset integrator 340 receives the scaled frequency error value $\hat{f}_{sc}$ and outputs a frequency offset value $f_{off}$ that characterizes the difference in frequency between the oscillators of the transmitter and receiver. In a preferred implementation, frequency offset integrator 340 is constructed as a perfect integrator as shown in FIG. 7. Assuming that the frequencies of the transmitter and receiver oscillators are perfectly constant and that the random component of the phase noise does not affect the DFLL, then one can see that the value of $\hat{f}_{sc}$ will approach zero and that the value of $f_{off}$ will approach a constant. The range of possible values for $f_{off}$ represents the range of frequency offsets that may be compensated by this circuit.

One of ordinary skill in the art will recognize that loop filters of higher order, such as the second-order configuration shown in FIG. 11, may be used instead of a first-order configuration for loop filter 325 if, for example, a different convergence characteristic is desired. In these alternative implementations of the invention, the structures of frequency offset integrators 340a and 340b will typically be the same as shown in FIG. 7 for integrator 340, and first scaler 330a and second scaler 330b may each have the same constant value or may have different constant values.

Phase adjustment integrator 350 serves to convert the frequency offset $f_{off}$ into a phase adjustment factor θ. In a preferred implementation, phase adjustment integrator 350 has either the structure shown in FIG. 8A or the one shown in FIG. 8B; the maximum and minimum values of output value θ substantially correspond to π and −π, respectively; and overflow is ignored such that phase adjustment integrator 350 performs modulo 2π accumulation.

Lookup table 360 is preprogrammed to convert the phase value θ into a pair of values representing a complex phase vector (for example, cos θ and sin θ). After passing through complex conjugator 370, this complex vector is input to phase rotator 220, where the pilot sample is rotated according to the following expression:

$r_p e^{j(p-\theta)} = r_p e^{jp} e^{-j\theta} = r_p (\cos p + j \sin p)(\cos \theta - j \sin \theta)$,

where $r_p$ is the magnitude of the pilot sample, p is the angle of the pilot sample as received, and p−θ is the angle of the pilot sample after correction of the frequency offset.

The rotated pilot samples are also input to pilot filter 160, which produces an estimate of the channel. The channel estimate represents the distortions of phase rotation and magnitude scaling introduced into the pilot signal by the channel and is typically reported as a vector in I/Q space. The number of taps N in filter 160 is chosen to provide the best overall channel estimate. On one hand, it is desirable that the channel remains relatively constant over the life span of the estimate, so that N should remain small. On the other hand, an estimate of higher accuracy may be obtained with a larger N. Filter 160 may be implemented as either an IIR or a FIR filter. In a preferred embodiment, filter 160 is an complex eight-tap rectangular averager.

Because the channel estimate is constructed from rotated pilot samples, its phase does not coincide with the phase of the samples in the data channel to be demodulated. Therefore, it is necessary to remove the rotation that was introduced by phase rotator 220 before this estimate may be applied to the data channel. Toward this end, the phase rotation factors that were supplied to phase rotator 220 by phase calculation block 250 are delayed by derotation delay 380 such that they reach phase derotator 240 at substantially the same time as the corresponding channel estimate is produced by pilot filter 160. As shown in FIG. 6, derotation delay 380 may receive the values θ from phase adjustment integrator 350. In a preferred implementation, however, as shown in FIG. 9, derotation delay 380 receives θ and also $f_{off}$, and a split-sample delay time is effectively obtained by combining these two values in an appropriate proportion.

Lookup table 390 is preprogrammed to convert the delayed phase value $\phi$ into a pair of values representing a complex phase vector (for example, cos $\phi$ and sin $\phi$). In a preferred implementation, lookup tables 360 and 390 are the same unit, and the addressing input to this table is multiplexed between phase adjustment integrator 350 and derotation delay 380. Note that if lookup tables 360 and 390 are not the same unit, then lookup table 360 may be modified to hold complex conjugate values instead, thereby dispensing with the need for complex conjugator 370.

The complex vector is input to phase derotator 240. As with phase rotator 220, the preferred implementation of phase derotator 240 is a complex multiplier as shown in FIG. 5. Because the phase adjustment vector is not complex conjugated in this stage, the rotation introduced by phase rotator 220 is removed from the channel estimate according to the following expression:

$$e^{j(p-\theta+\phi} = e^{j(p-\theta)}e^{j\phi} = [(\cos p + j \sin p)\ (\cos \theta - j \sin \theta)]\ (\cos \phi + j \sin \phi),$$

where $p-\theta$ is the angle of the channel estimate, and $p-\theta+\phi$ is the angle of the channel estimate after restoration of the frequency offset. In a preferred implementation, the derotation angle $\phi$ has the same value as the rotation angle $\theta$, so that the value of $p-\theta+\phi$ is simply p, the angle of the pilot sample as received. However, it is also possible to refine the value of $\phi$ on the basis of information that was not available when the value of $\theta$ was calculated.

After derotation, the channel estimate passes through complex conjugator 170 and is combined with the despread and delayed data samples in coherent detector 190. As with phase rotator 220 and derotator 240, the preferred implementation of coherent detector 190 is a complex multiplier as shown in FIG. 5.

In the preferred embodiments described and illustrated above, the phase rotation $\theta$ is calculated from a first set of pilot samples, taken at a first point in time from the stream of samples output by PN despreader 115. In phase rotator 220, the phase rotation $\theta$ is then applied to a second set of pilot samples, taken from the same stream of samples output by PN despreader 115 but at a later point in time than the first set. In an alternative embodiment, as shown in FIG. 12, the phase rotation $\theta$ calculated from a set of pilot samples is applied in phase rotator 220 back to the same set of pilot samples by, for example, keeping a copy of each set of pilot samples in a buffer 260.

The foregoing description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles presented herein may be applied to

other embodiments without use of the inventive faculty. For example, even though the preferred embodiment relates to a CDMA receiver with a code-division-multiplexed pilot, the invention may also be applied to a receiver with a time-division-multiplexed pilot or to a TDMA receiver. Additionally, one of ordinary skill in the art will recognize that although the preferred embodiment of the invention processes signals that have been digitized, the novel principles described herein are equally applicable to a system that processes analog signals or to a hybrid system. Thus, the present invention is not intended to be limited to the embodiments shown above, but rather is to be accorded the widest scope consistent with the principles and novel features disclosed in any fashion herein.

What is claimed is:

# CLAIMS

1. A method for frequency offset correction, comprising:
determining a frequency offset within a pilot;
phase-rotating the pilot according to the frequency offset;
filtering the pilot to obtain a channel estimate; and
derotating the channel estimate to restore the frequency offset.

2. A method for frequency offset correction, comprising:
despreading a first plurality of pilot samples to obtain a first plurality of despread pilot samples;
despreading a second plurality of pilot samples to obtain a second plurality of despread pilot samples;
determining a frequency offset within the first plurality of despread pilot samples;
phase-rotating the second plurality of despread pilot samples to compensate for the frequency offset;
filtering the second plurality of despread pilot samples to obtain a channel estimate; and
derotating the channel estimate to restore the frequency offset,
wherein the first plurality of pilot samples is taken from a stream of samples at a first point in time and the second plurality of pilot samples is taken from the stream of samples at a second point in time.

3. The method of claim 2, wherein filtering the second plurality of despread pilot samples to obtain a channel estimate comprises passing the second plurality of pilot samples through a lowpass filter.

4. The method of claim 2, wherein filtering the second plurality of despread pilot samples to obtain a channel estimate comprises averaging the second plurality of pilot samples.

5. The method of claim 2, wherein despreading a second plurality of pilot samples to obtain a second plurality of despread pilot samples comprises passing the second plurality of pilot samples through an integrate-and-dump filter.

6. The method of claim 2, wherein despreading a first plurality of pilot samples to obtain a first plurality of despread pilot samples comprises passing the first plurality of pilot samples through an integrate-and-dump filter.

7. The method of claim 6, wherein despreading a second plurality of pilot samples to obtain a second plurality of despread pilot samples comprises passing the second plurality of pilot samples through an integrate-and-dump filter.

8. An apparatus for frequency offset correction, comprising:

a phase rotator receiving a pilot and a first phase adjustment value and outputting a rotated pilot, the pilot having a frequency offset and a phase rotation;

a frequency discriminator receiving the rotated pilot and outputting a frequency error value;

a phase calculation and delay unit receiving the frequency error value and outputting the first phase adjustment value and a second phase adjustment value;

a pilot filter receiving the rotated pilot and outputting a channel estimate; and

a phase derotator receiving the channel estimate and the second phase adjustment value and outputting a derotated channel estimate,

wherein the first and second phase adjustment values are complex values, and

wherein the second phase adjustment value is substantially a delayed version of the first phase adjustment value, and

wherein the rotated pilot is substantially the pilot without the frequency offset, and

wherein the channel estimate is substantially a complex value representing the phase rotation.

9. An apparatus according to claim 8, said frequency discriminator comprising a quadricorrelator.

10. An apparatus according to claim 8, said phase calculation and delay unit comprising:

a first integrator receiving a signal based on the frequency error value and outputting a frequency offset value; and

a second integrator receiving the frequency offset value and outputting a phase correction value;

wherein the first phase adjustment value and the second phase adjustment value are based on the phase correction value.

11. An apparatus for frequency offset correction, comprising:

a pilot despreader receiving a plurality of received pilot samples and outputting a plurality of despread pilot samples, said plurality of despread pilot samples having a frequency offset and a phase rotation;

a phase rotator receiving the plurality of despread pilot samples and a first phase adjustment value and outputting a first plurality of rotated pilot samples;

a frequency discriminator receiving a second plurality of rotated pilot samples and outputting a frequency error value;

a phase calculation and delay unit receiving the frequency error value and outputting the first phase adjustment value and a second phase adjustment value;

a pilot filter receiving the first plurality of rotated pilot samples and outputting a channel estimate; and

a phase derotator receiving the channel estimate and the second phase adjustment value and outputting a derotated channel estimate,

wherein the first and second phase adjustment values are complex values, and

wherein the second phase adjustment value is substantially a delayed version of the first phase adjustment value, and

wherein the second plurality of rotated pilot samples is substantially the plurality of despread pilot samples without the frequency offset, and

wherein the channel estimate is substantially a complex value representing the phase rotation, and

wherein the second plurality of rotated pilot samples is derived from a plurality of samples taken from a stream of samples at a first point in time, and the plurality of received pilot samples is taken from the stream of samples at a second point in time.

12. An apparatus according to claim 11, said frequency discriminator comprising a quadricorrelator.

13. An apparatus according to claim 11, said phase calculation and delay unit comprising:

a first integrator receiving a signal based on the frequency error value and outputting a frequency offset value; and

a second integrator receiving the frequency offset value and outputting a phase correction value,

wherein the first phase adjustment value and the second phase adjustment value are based on the phase correction value.

14. An apparatus according to claim 11, wherein the second phase adjustment value is substantially a delayed and conjugated version of the first phase adjustment value.

15. An apparatus according to claim 11, said pilot despreader comprising an integrate-and-dump filter.

16. An apparatus according to claim 11, said pilot filter comprising a lowpass filter.

17. An apparatus according to claim 11, said pilot filter comprising a finite-impulse-response filter.

18. An apparatus according to claim 11, said pilot filter comprising an averager.

19. An apparatus according to claim 11, said second phase adjustment value being delayed by substantially one-half of a group delay of said pilot filter.

20. An apparatus according to claim 11, said second phase adjustment value being delayed by a time which is not an integer multiple of a sample time of said plurality of despread pilot samples.

21. An apparatus for frequency offset correction, comprising:

a plurality of phase rotators each receiving a first phase adjustment value and one of a plurality of pilots and outputting a corresponding one of a plurality of rotated pilots, each of the pilots having a frequency offset and a phase rotation;

a plurality of frequency discriminators each receiving one of the rotated pilots and outputting a corresponding one of a plurality of frequency error values;

a phase calculation and delay unit receiving the plurality of frequency error values and outputting the first phase adjustment value and a second phase adjustment value;

a plurality of pilot filters each receiving one of the rotated pilots and outputting a corresponding one of a plurality of channel estimates; and

a plurality of phase derotators each receiving the second phase adjustment value and one of said plurality of channel estimates and outputting a corresponding one of a plurality of derotated channel estimates,

wherein the first and second phase adjustment values are complex values, and

wherein the second phase adjustment value is substantially a delayed version of the first phase adjustment value, and

wherein each of the rotated pilots is substantially a corresponding one of the pilots without the frequency offset, and

wherein each of the plurality of channel estimates is substantially a complex value representing the phase rotation of a corresponding one of the pilots.

22. An apparatus according to claim 21, at least one among said plurality of frequency discriminators comprising a quadricorrelator.

23. An apparatus for frequency offset correction, comprising:

a plurality of pilot despreaders each receiving one of a plurality of sets of received pilot samples and outputting a corresponding one of a plurality of sets of despread pilot samples, each of the plurality of sets of despread pilot samples having a frequency offset and a phase rotation;

a plurality of phase rotators each receiving a first phase adjustment value and one of the plurality of sets of despread pilot samples and outputting a corresponding one of a plurality of first sets of rotated pilot samples;

a plurality of frequency discriminators each receiving one of a plurality of second sets of rotated pilot samples and outputting a corresponding one of a plurality of frequency error values;

a phase calculation and delay unit receiving the plurality of frequency error values and outputting the first phase adjustment value and a second phase adjustment value;

a plurality of pilot filters each receiving one of the plurality of first sets of rotated pilot samples and outputting a corresponding one of a plurality of channel estimates; and

a plurality of phase derotators each receiving the second phase adjustment value and one of the plurality of channel estimates and outputting a corresponding one of a plurality of derotated channel estimates,

wherein the first and second phase adjustment values are complex values, and

wherein the second phase adjustment value is substantially a delayed version of the first phase adjustment value, and

wherein each of the plurality of second sets of rotated pilot samples is substantially a corresponding one of the plurality of sets of despread pilot samples without the frequency offset, and

wherein each of the plurality of channel estimates is substantially a complex value representing the phase rotation of a corresponding one of the plurality of sets of despread pilot samples, and

wherein each of the plurality of second sets of rotated pilot samples is derived from a plurality of samples taken from a corresponding one of a plurality of streams of samples at a corresponding one of a plurality of first points in time, and

wherein each of the plurality of sets of received pilot samples is taken from a corresponding one of the plurality of streams of samples at a corresponding one of a plurality of second points in time.

24. An apparatus according to claim 23, at least one among said plurality of frequency discriminators comprising a quadricorrelator.

25. An apparatus according to claim 24, wherein the pilot has a magnitude scaling, and

wherein the channel estimate is substantially a complex value representing the magnitude scaling.

26. An apparatus according to claim 11, wherein the plurality of despread pilot samples has a magnitude scaling, and

wherein the channel estimate is substantially a complex value representing the magnitude scaling.

27. An apparatus according to claim 2, wherein the first and second pluralities of pilot samples are the same, and the first and second points in time are the same.

28. An apparatus for frequency offset correction, comprising:

a pilot despreader receiving a plurality of received pilot samples and outputting a plurality of despread pilot samples, said plurality of despread pilot samples having a frequency offset and a phase rotation;

a buffer receiving the plurality of despread pilot samples and outputting a plurality of delayed despread pilot samples;

a phase rotator receiving the plurality of delayed despread pilot samples and a first phase adjustment value and outputting a plurality of rotated pilot samples;

a frequency discriminator receiving the plurality of despread pilot samples and outputting a frequency error value;

a phase calculation and delay unit receiving the frequency error value and outputting the first phase adjustment value and a second phase adjustment value;

a pilot filter receiving the plurality of rotated pilot samples and outputting a channel estimate; and

a phase derotator receiving the channel estimate and the second phase adjustment value and outputting a derotated channel estimate,

wherein the first and second phase adjustment values are complex values, and

wherein the second phase adjustment value is substantially a delayed version of the first phase adjustment value, and

wherein the plurality of rotated pilot samples is substantially the plurality of despread pilot samples without the frequency offset, and

wherein the channel estimate is substantially a complex value representing the phase rotation.

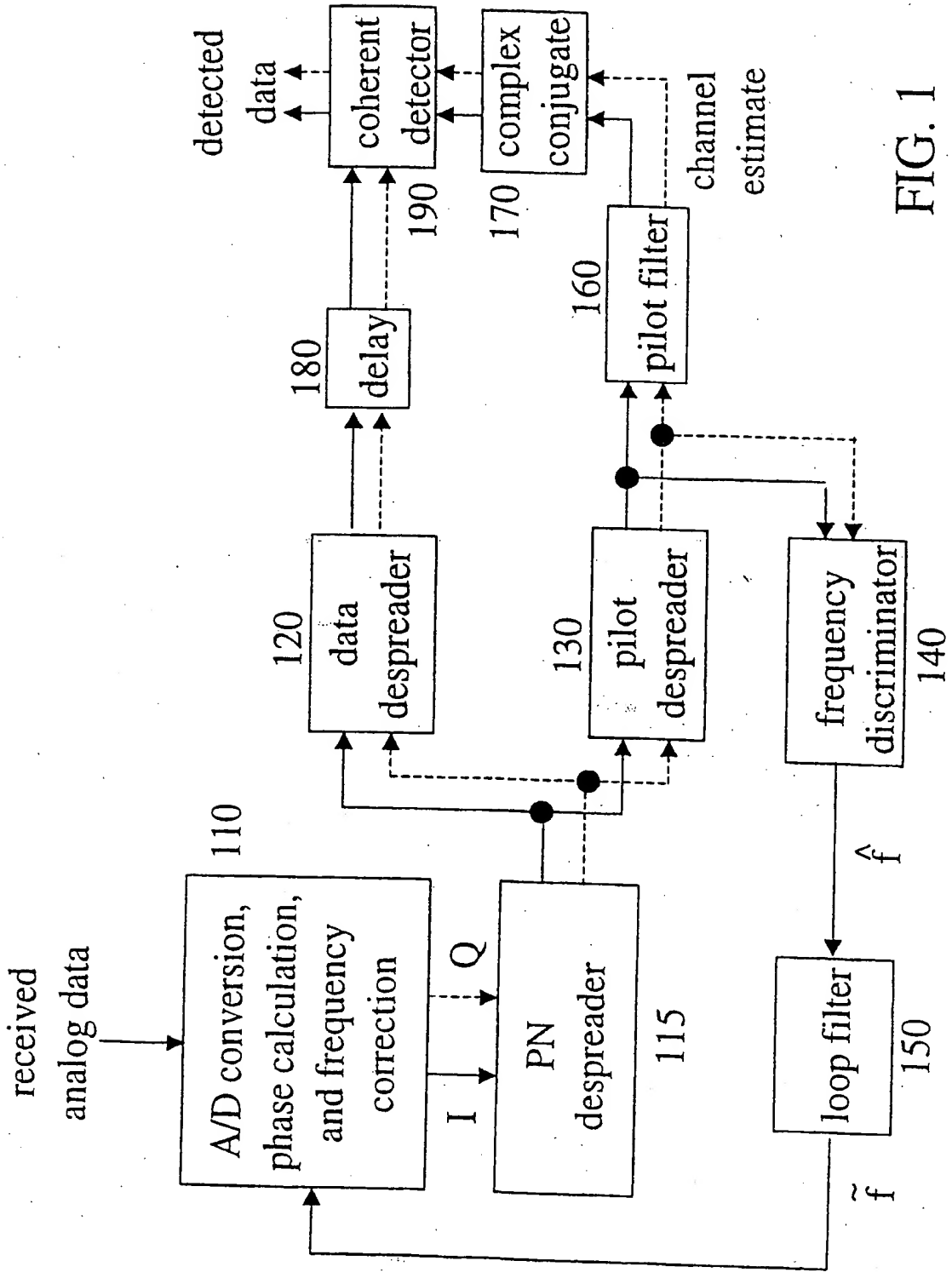

received analog data
A/D conversion, phase calculation, and frequency correction
110
I
Q
PN despreader
115
data despreader
120
pilot despreader
130
frequency discriminator
140
loop filter
150
pilot filter
160
complex conjugate
170
coherent detector
190
delay
180
detected data
channel estimate
f̂
f̃

FIG. 1

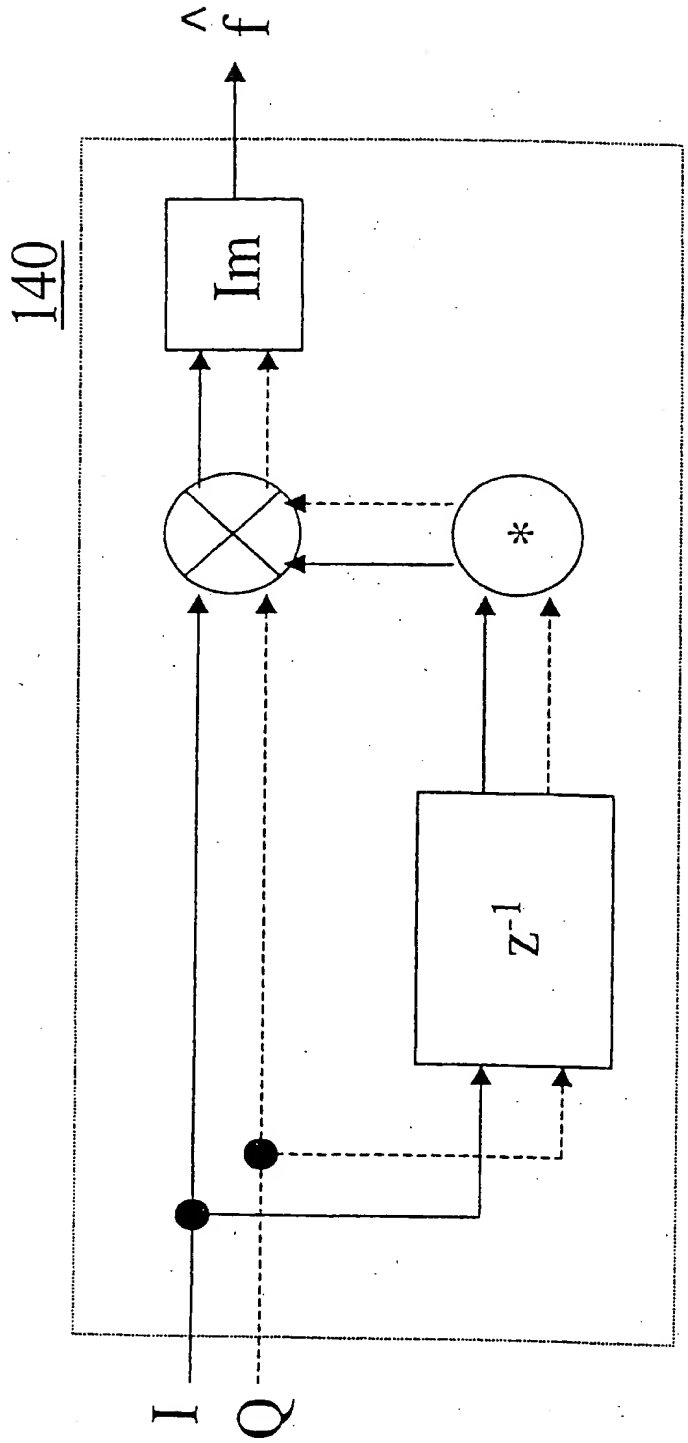
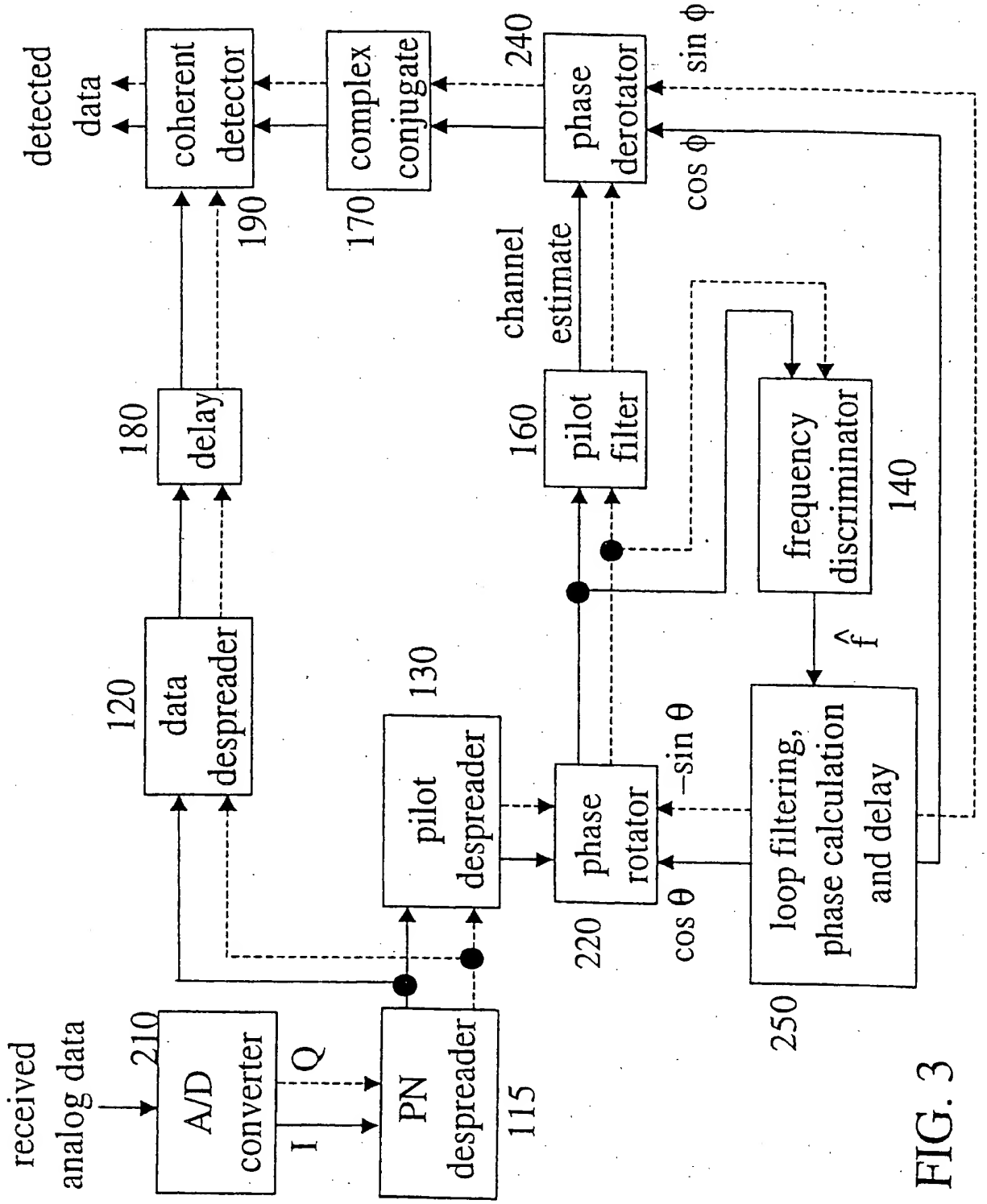



FIG. 2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210
A/D converter
I
Q
PN despreader
115
pilot despreader
130
data despreader
120
delay
180
coherent detector
190
detected data
complex conjugate
170
phase rotator
220
cos θ
−sin θ
pilot filter
160
channel estimate
phase derotator
240
cos ϕ
sin ϕ
frequency discriminator
140
f̂
loop filtering, phase calculation and delay
250

FIG. 3

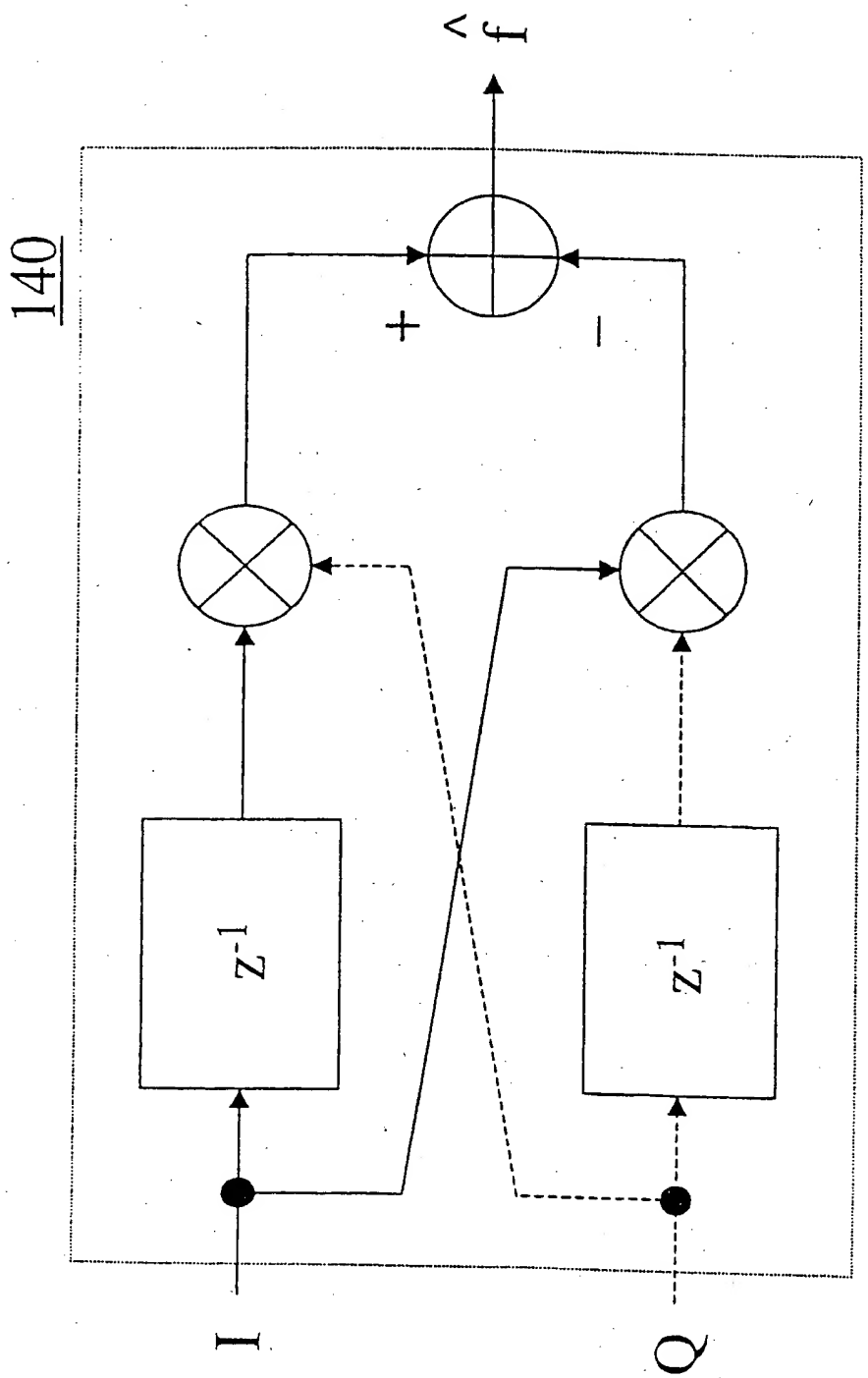


FIG. 4

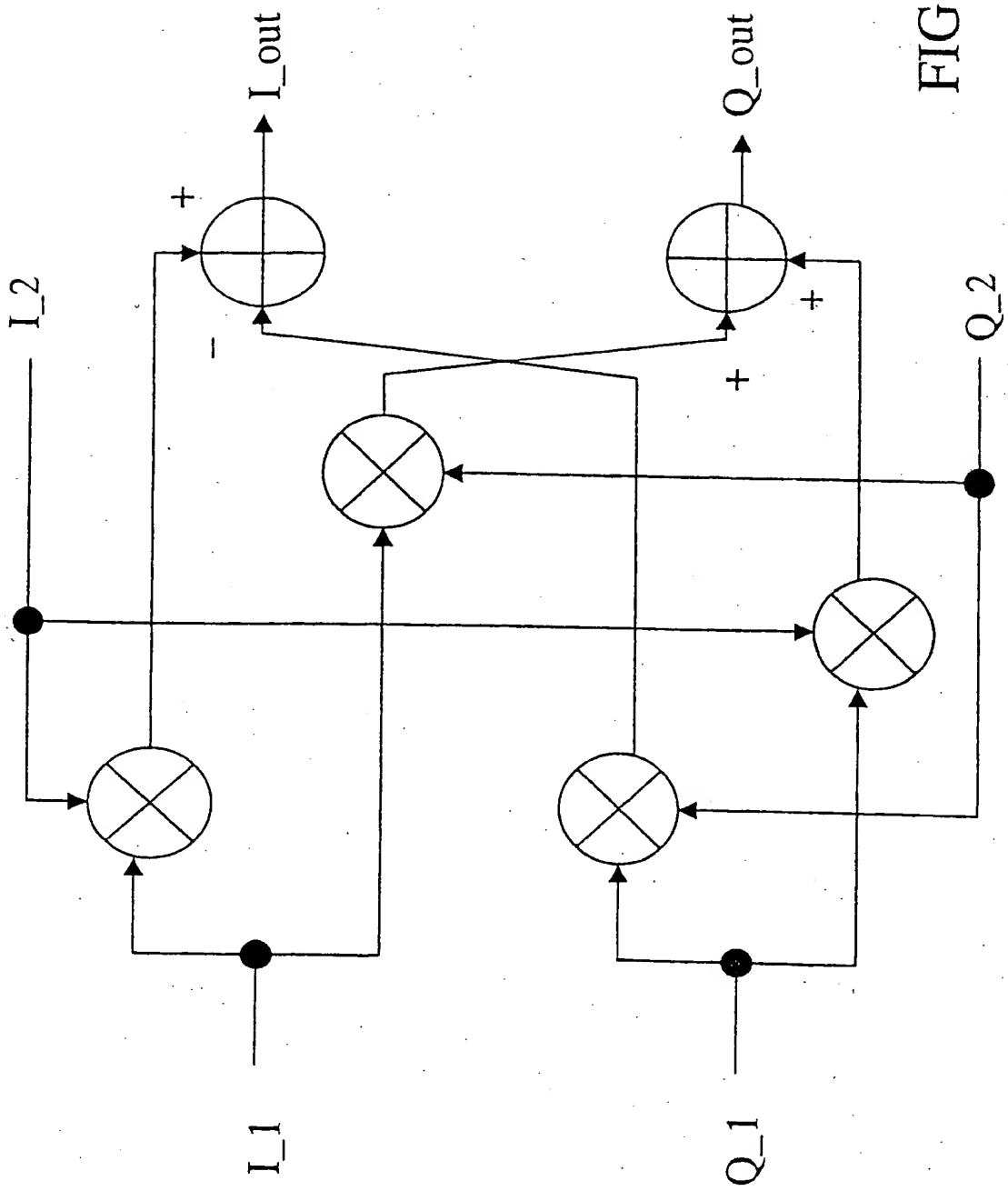


FIG. 5

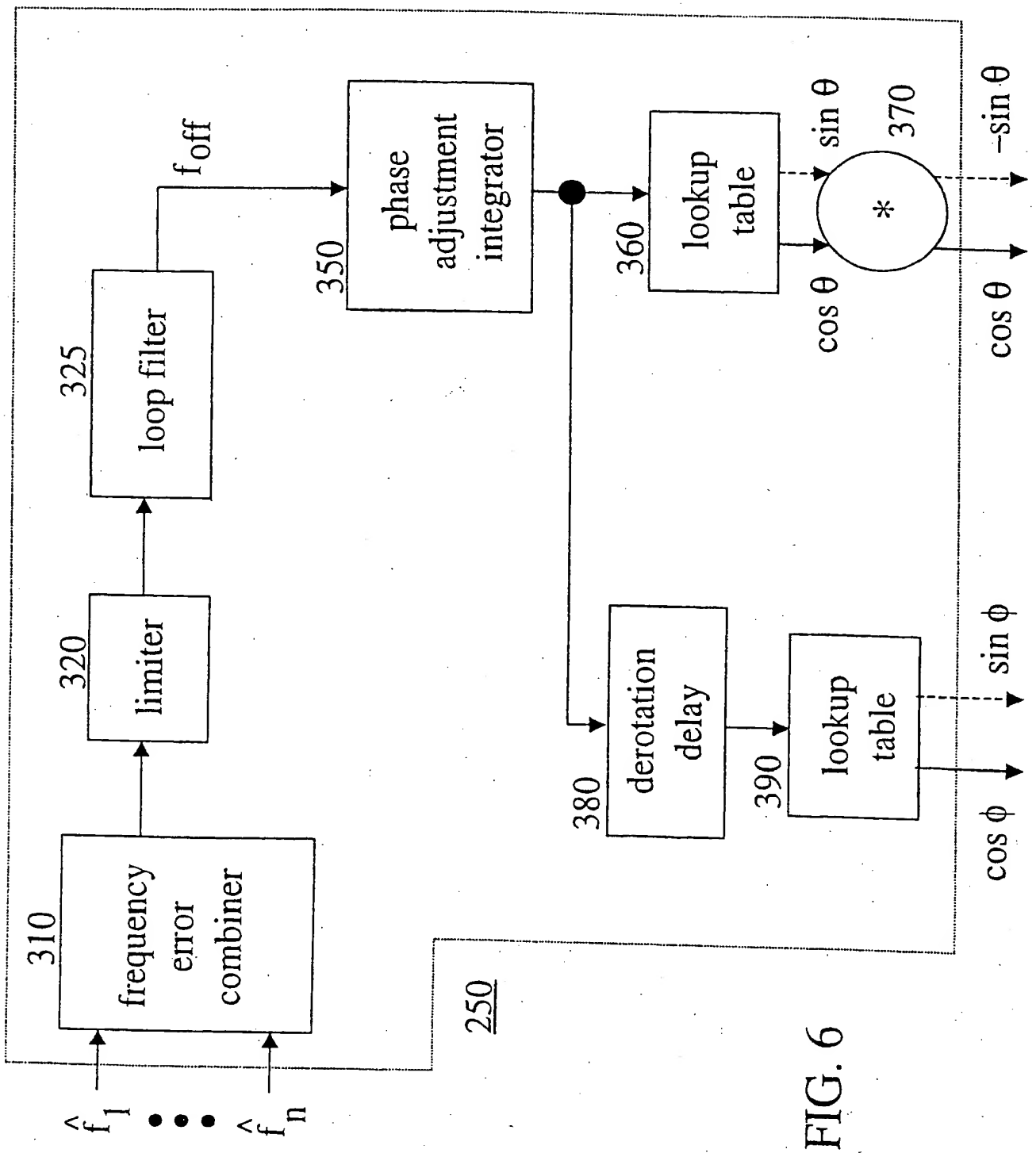
$\hat{f}_1$
$\hat{f}_n$
310
frequency error combiner
320
limiter
325
loop filter
$f_{off}$
350
phase adjustment integrator
360
lookup table
sin θ
cos θ
370
*
−sin θ
cos θ
380
derotation delay
390
lookup table
sin ϕ
cos ϕ
250

FIG. 6

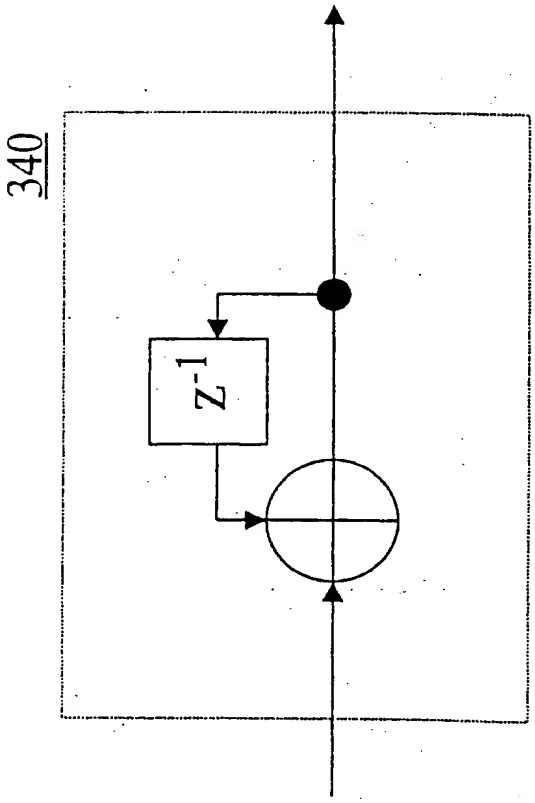


FIG. 7

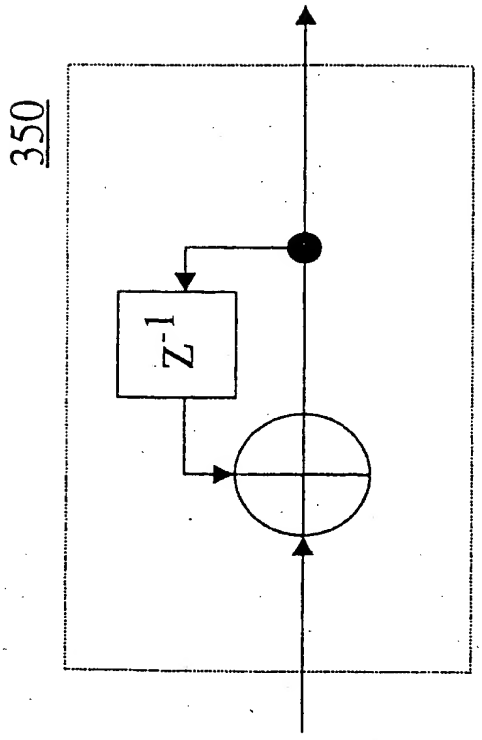


FIG. 8A

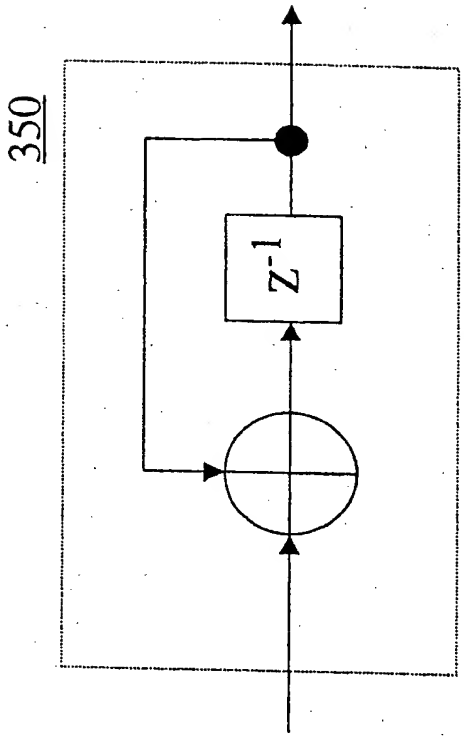


FIG. 8B

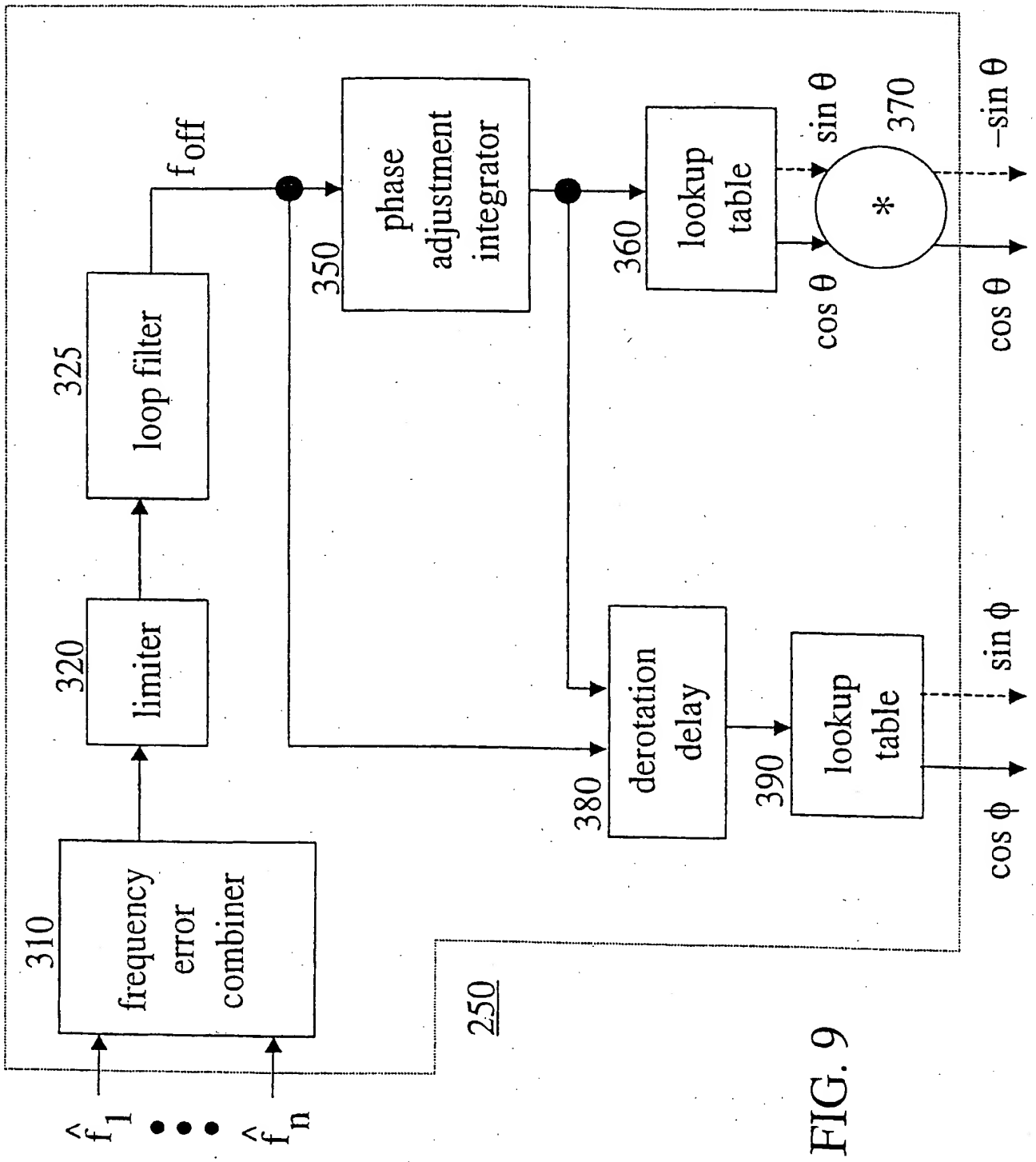
250
310
frequency error combiner
320
limiter
325
loop filter
$f_{off}$
350
phase adjustment integrator
360
lookup table
sin θ
cos θ
370
*
−sin θ
cos θ
380
derotation delay
390
lookup table
sin ϕ
cos ϕ
$\hat{f}_1$
$\hat{f}_n$

FIG. 9

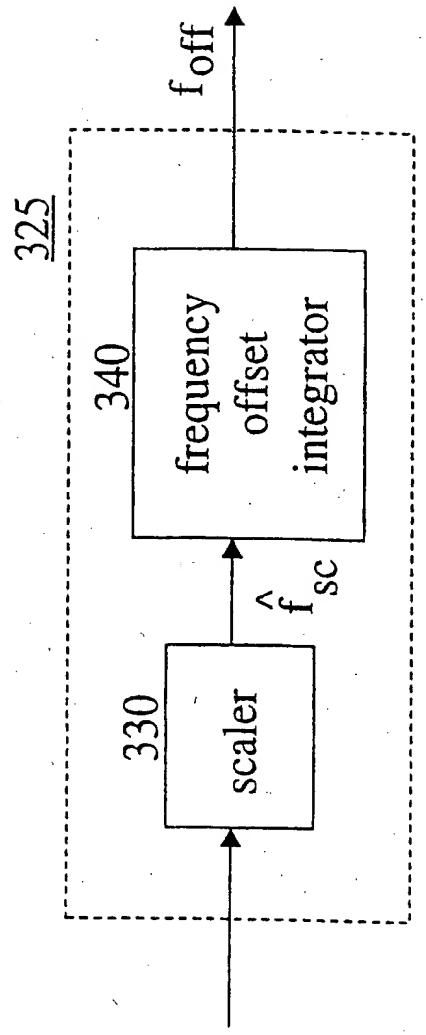
$f_{off}$
325
340
frequency offset integrator
$\hat{f}_{sc}$
330
scaler

FIG. 10

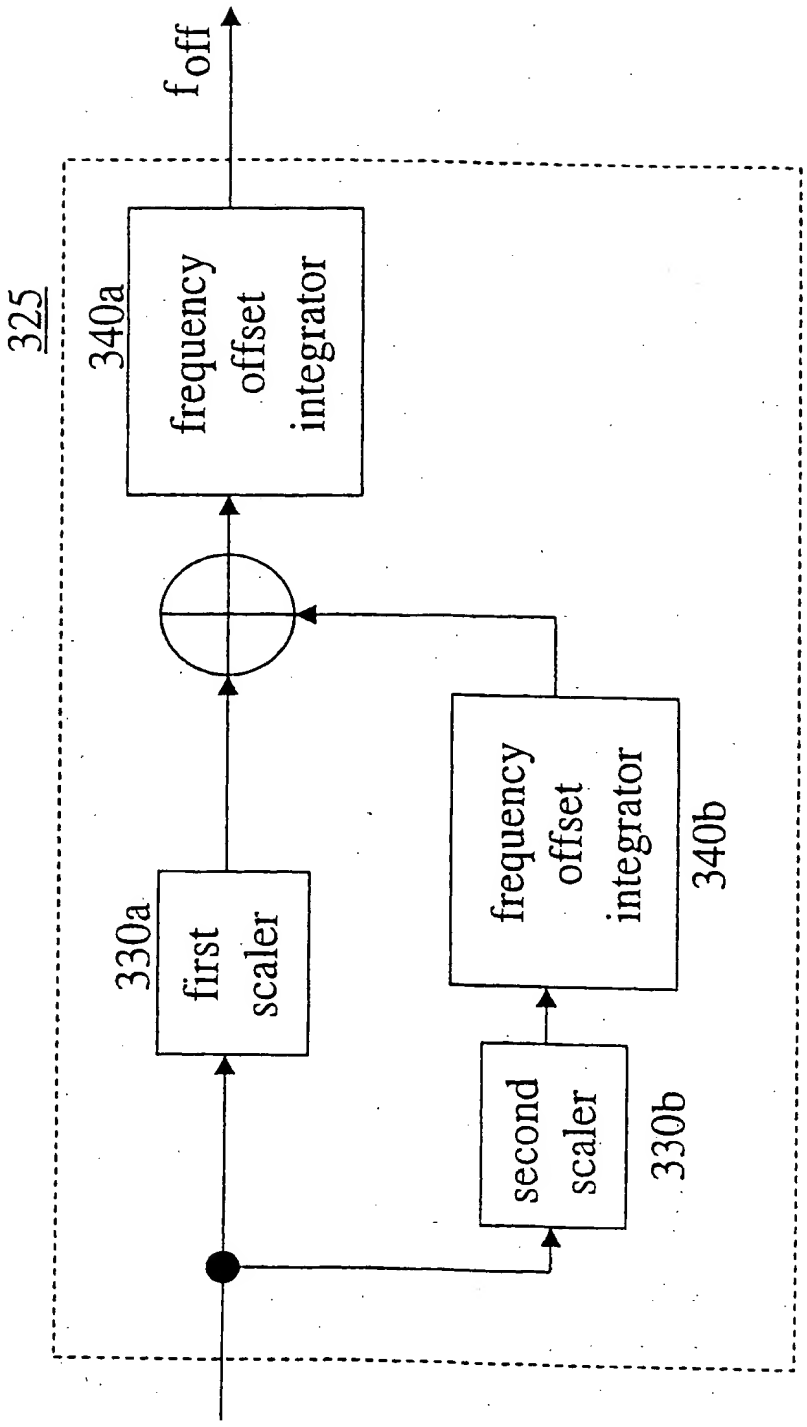
$f_{off}$
325
340a
frequency offset integrator
330a
first scaler
frequency offset integrator
340b
second scaler
330b

FIG. 11

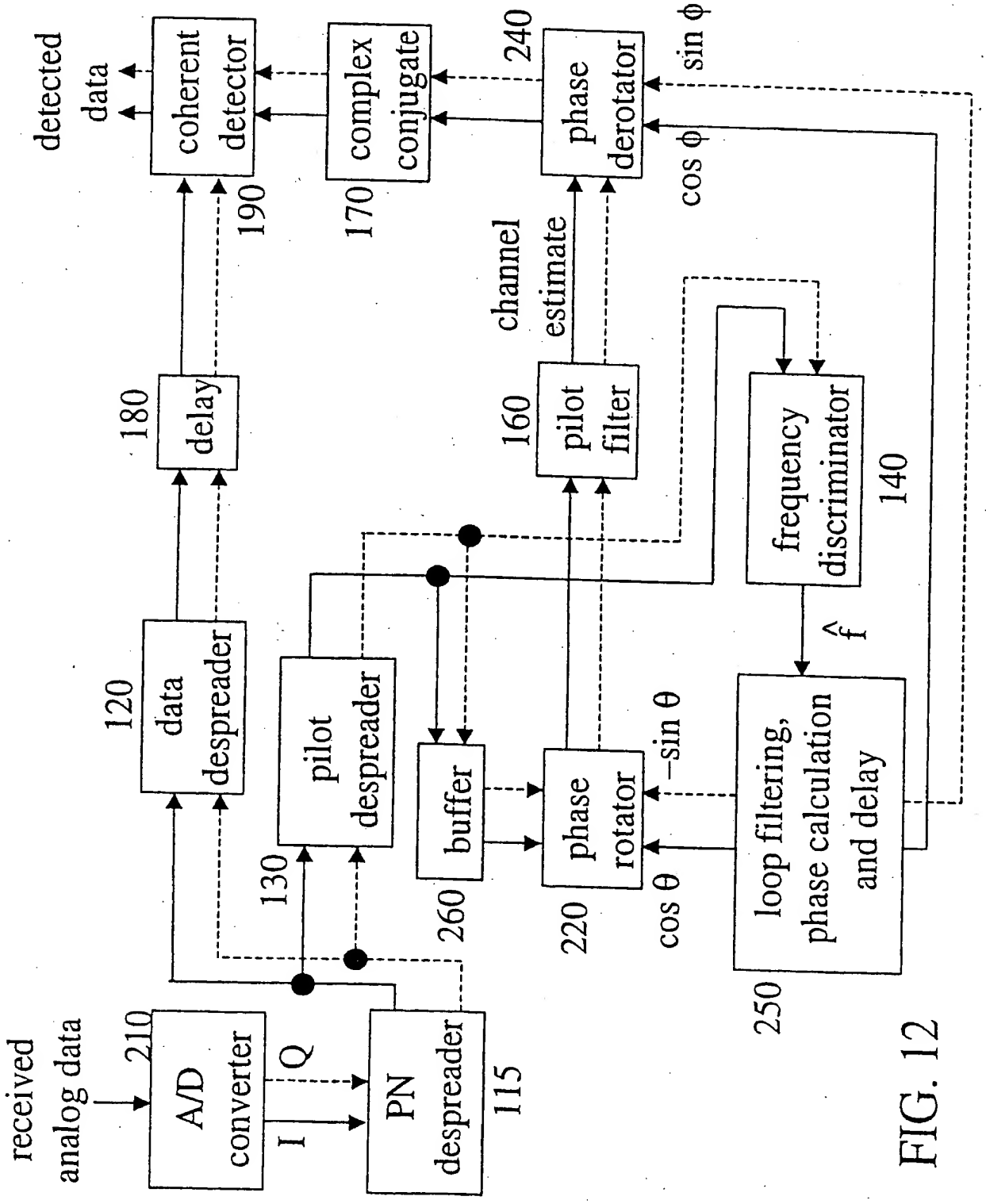
received analog data
210
A/D converter
I
Q
PN despreader
115
data despreader
120
pilot despreader
130
buffer
260
phase rotator
220
−sin θ
cos θ
loop filtering, phase calculation and delay
250
f̂
frequency discriminator
140
pilot filter
160
channel estimate
delay
180
coherent detector
190
detected data
complex conjugate
170
phase derotator
240
cos ϕ
sin ϕ

FIG. 12

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/10743

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L27/233 H04L25/02 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 5 619 524 A (BRUCKERT GENE ET AL)<br>8 April 1997 (1997-04-08)<br>column 7, line 31 - line 52<br>column 8, line 8 - line 12<br>column 8, line 21 - line 28<br>column 8, line 46 - line 49<br>--- | 1-28 |
| A | WO 98 40991 A (INTERDIGITAL TECH CORP)<br>17 September 1998 (1998-09-17)<br>page 9, line 5 - line 9<br>page 10, line 19 -page 11, line 7<br>--- | 1-28 |
| A | EP 0 898 379 A (MATSUSHITA ELECTRIC IND CO LTD) 24 February 1999 (1999-02-24)<br>page 4, line 37 - line 56<br>--- | 1-28 |

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 3 August 2000 | 10/08/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P B 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel (-31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax (-31-70) 340-3016 | Orozco Roura, C |

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# INTERNATIONAL SEARCH REPORT

Inte. .ational Application No
PCT/US 00/10743

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication.where appropriate. of the relevant passages | Relevant to claim No. |
|---|---|---|
| P,X | WO 99 31816 A (ERICSSON GE MOBILE INC)<br>24 June 1999 (1999-06-24)<br>page 3, line 19 - line 30<br>page 5, line 30 -page 6, line 7<br>page 11, line 27 - line 31<br>----- | 1-28 |

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte.. ational Application No
PCT/US 00/10743

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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| EP 0898379 A | 24-02-1999 | JP 11068698 A | 09-03-1999 |
| | | CA 2237827 A | 20-02-1999 |
| | | CN 1209003 A | 24-02-1999 |
| WO 9931816 A | 24-06-1999 | AU 1710499 A | 05-07-1999 |